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(54) **Frequency synthesizer**

Frequenzsynthesizer

Synthétiseur de fréquence

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Description

BACKGROUND OF THE INVENTION

1.Field of the Invention

[0001] The present invention generally relates to a frequency synthesizer used in a wireless mobile appliance, and more specifically, to a frequency synthesizer capable of manufacturing a VCO in an IC form, resulting in low cost.

2.Description of the Related Art

[0002] In wireless mobile appliances such as portable telephones, frequency synthesizers are used to generate arbitrary local oscillation frequencies from a reference signal.

[0003] In general, as indicated in Fig. 5, a frequency synthesizer used in a wireless mobile appliance such as a portable telephone is equipped with a VCO 1, a prescaler 2, a counter 3, a reference frequency divider 5, a phase comparator 6, a charge pump 7, and a loop filter 8. Both the prescaler 2 and the counter 3 constitute a pulse-swallow type variable frequency divider. The VCO 1 oscillates a signal having a frequency in response to a voltage which is applied to a frequency control voltage terminal of the frequency synthesizer. The prescaler 2 divides a frequency of an output signal (will be referred to as an "f_{VCO}" hereinafter) of the VCO 1. The counter 3 counts the output signal of the prescaler 2. The reference frequency divider 5 divides a frequency of an output signal (will be referred to as an "f_{OSC}" hereinafter) of a reference signal source 4. The phase comparator 6 compares a phase of an output signal (will be referred to as an "f_{div}" hereinafter) of the counter 3 with a phase of an output signal (will be referred to as an "f_{ref}" hereinafter) of the reference frequency divider 5 to thereby output a phase difference. The charge pump 7 converts the output signal of the phase comparator 6 into either a voltage or a current. The loop filter 8 averages the output signal of the charge pump 7.

[0004] Fig. 6 is a circuit diagram for representing a basic operation of the VCO disclosed in Japanese Laid-open Patent Application No. Hei-10-261918. This circuit is provided with the capacitor "CO", the negative-characteristic resistive portion "-R", and the inductor "L", which are connected in parallel to each other. This circuit is further equipped with the capacitor "C1" and the variable capacitance diode "Cv", which are connected in the cascade connection. This cascade connection between the capacitor C1 and the variable capacitance diode "Cv" is connected in parallel to the capacitor CO.

[0005] Next, operations of the circuit shown in Fig. 6 will now be explained. The parallel connection portion constructed of the negative-characteristic resistive portion "-R", the capacitor "CO", and the inductor "L" corresponds to a parallel resonant circuit containing an active element which generates electric power of a transistor and the like, to which the power supply voltage is applied. The negative-characteristic resistive portion "-R" is different from the normal resistor, considering such an implication that electric power is generated.

[0006] The oscillation frequency of this VCO is expressed by the following formula [1]:

$$f_{VCO} = 1/2\ \pi\sqrt{L[C0+C1 \cdot Cv/(C1+Cv)]} \qquad [1]$$

[0007] In the case that this voltage-controlled oscillator is employed in the frequency synthesizer of Fig. 5, the control voltage is applied to the variable capacitance diode "Cv", so that the capacitance value of the variable capacitance diode "Cv" is varied. As a result, the oscillation frequency "fvco" is varied.

[0008] In such a frequency synthesizer, when the count value of the counter 3 is changed, the frequency "f_{div}" is changed in response to this change in the count values. As a result, the phase comparator 6 outputs the phase error. Based upon this phase error, voltage of the frequency control voltage terminal of the VCO 1 is changed via the charge pump 7 and the loop filter 8 so as to vary the frequency "f_{VCO}." As previously explained, the frequency synthesizer constitutes the negative feedback loop, and finally locks the phase when the phase of the frequency "f_{ref}" is made coincident with the phase of the frequency "f_{div}", so that the output frequency of the VCO 1 can be made stable.

[0009] Generally speaking, in such a frequency synthesizer, a VCO is constituted by a module component. This module component will constitute one of major factors which may impede a compactness of a portable telephone and the like. Thus, such a VCO is desirably manufactured in the form of an IC component. However, in the case that such a VCO is manufactured in the IC component form, an oscillation frequency of this VCO would be largely varied due to manufacturing fluctuations occurred in electronic components for constituting this VCO. As a result, there is such a problem that the frequency synthesizer could not be phase-locked at the desirable frequency.

[0010] To solve this problem, there is one method capable of increasing a control sensitivity (namely, change width

of oscillation frequency per 1V : unit being [Hz/V]). However, if the control sensitivity is increased, then there is another problem. That is, when the control sensitivity is increased, the frequency synthesizer may be easily and adversely influenced by outer disturbance noise, so that the CPU characteristic would be deteriorated.

[0011] Also, there is a further method for solving the above-explained problem. That is, in this method, a plurality of fixed capacitances are connected in parallel to a parallel resonant circuit of a VCO, and when this VCO is manufactured in the IC component form, these fixed capacitances are trimmed by laser and the like so as to set the oscillation frequency of the VCO. However, since the IC is separately adjusted, the manufacturing cost would be increased, resulting in another problem.

[0012] Document EP 0 910 170 A2 describes a self calibrating phase-lock loop (PLL) which has an oscillator having a plurality of operating curves. During PLL auto-trim operations, the oscillator is automatically trimmed to' an appropriate oscillator operating curve for use during normal PLL operations. During the PLL auto-trim operations, a state machine applies a sequence of digital control input values to the VCO to select different VCO operating curves until an appropriate operating curve for the present PLL application is found.

[0013] An electronic device having a frequency synthesizer and a method for controlling its frequency is presented in document EP 0 944 171 A1. The frequency synthesizer comprises a PLL and a VCO having a plurality of capacitors. Its frequency is controlled by connecting/disconnecting capacitors to/from the VCO circuitry in dependence of a frequency error detected by frequency adjusting means.

[0014] Document GB 2 282 285 A shows a frequency synthesizer having a VCO and which oscillates over a wide frequency band even if change of oscillation frequency due to change of the control voltage is small. This is achieved by changings an capacitance component of the VCO separately from the control using the control voltage.

SUMMARY OF THE INVENTION

[0015] The present invention has been made to solve the above-described conventional problems, and therefore, has an object to provide a frequency synthesizer having a better C/N characteristic, by which a VCO having a wide output frequency range can be manufactured in an IC form, while realizing low cost.

[0016] This is achieved by the features as set forth in the independent claims.

[0017] A frequency synthesizer which achieves the above-explained object is featured by that, it having a switching means for switching a capacitor, or an inductor; and is equipped with: a voltage-controlled oscillator (will be referred to as a "VCO" hereinafter) for oscillating a signal having a frequency in response to a voltage applied to a control voltage terminal; a first frequency divider for outputting a signal having a frequency which is obtained by dividing a frequency of an output signal derived from the VCO; a second frequency divider for dividing a frequency of a reference signal; a phase comparator for comparing a phase of an output signal of the first frequency divider with a phase of an output signal of the second frequency divider to output a phase difference thereof; and a charge pump for outputting the output signal of the phase comparator via a loop filter to a control voltage terminal of the VCO,

the frequency synthesizer is comprised of: frequency adjusting means for detecting a frequency error between both the output signal of the first frequency divider and the output signal of the second frequency divider, and for switching the capacitor value of the VCO, or the inductor value thereof in accordance with the detection result of the frequency error; and bias control means for applying an arbitrary voltage to the control voltage terminal of the VCO in order that the output signal of the charge pump is brought into a high impedance state when the frequency adjusting means is operated. With employment of such an arrangement, even when there is a manufacturing fluctuation occurred in the electronic components which constitute the VCO, since the resonant frequency of the parallel resonant circuit is varied in response to the actual oscillation frequency of the VCO, the phase can be locked at a desirable frequency. Furthermore, since the VCO can be manufactured in the IC form, the VCO can be made compact as well as in low cost.

[0018] Also, the frequency synthesizer is featured by that the VCO is equipped with a plurality of means for switching capacitors, or inductors. With employment of this arrangement, since the resonant frequencies are switched in a fine mode, the control sensitivity of the VCO can be lowered, and thus, the C/N characteristic can be improved.

[0019] Further, the frequency synthesizer is featured by comprising: first and second counters for counting the output signal of the first frequency divider and the output signal of the second frequency divider as a clock; time difference detecting means for detecting a time difference when the first counter produces a count end signal and the second counter produces a count end signal by employing a signal generated from the output signal of the VCO; and VCO control data producing means for producing a signal used to switch the capacitor value of the VCO, or the inductor value thereof in response to the output signal of the time difference detecting means. With employment of such an arrangement, since the frequency of the output signal of the first frequency divider is compared with the frequency of the output signal of the second frequency divider to switch the resonant circuits of the VCO, the phase can be locked at a desirable frequency even in such a case that the first frequency divider is such a frequency divider employed in the fractional N type frequency synthesizer in which the phase of the output signal is instantaneously changed.

[0020] Then, the frequency synthesizer is featured by comprising: first and second counters for counting the output

signal of the first frequency divider and the output signal of the second frequency divider as a clock; time difference detecting means for detecting a time difference when the first counter produces a count end signal and the second counter produces a count end signal by employing a signal generated from the output signal of the reference signal source; and VCO control data producing means for producing a signal used to switch the capacitor value of the VCO, or the inductor value thereof in response to the output signal of the time difference detecting means. With employment of such an arrangement, since the signal used to detect the time difference is constant irrespective of the oscillation frequency of the VCO, the precision in detecting of the time difference can be continuously kept constant.

[0021] Also, the frequency synthesizer is featured by comprising: a time difference judging means for resetting both the first counter and the second counter in response to the detection signal of the time difference detecting means, and for applying an arbitrary voltage to the control voltage terminal of the VCO so as to bring the output signal of the charge pump into the high impedance state in the case that the time difference detected by the time difference detecting means becomes a value defined within a predetermined time difference. With employment of such an arrangement, since the PLL is set to the closed loop after the frequency synthesizer confirms that the oscillation frequency of the VCO is approached to the desirable oscillation frequency, this frequency synthesizer can be phase-locked at the desirable oscillation frequency by using the optimum VCO control data.

[0022] Further, the frequency synthesizer is featured by comprising: a loop filter control means for outputting a signal causing a time constant of the loop filter to be varied in response to the output signal of the VCO control data producing means. With employment of such an arrangement, even when the control sensitivity of the VCO is varied in response to the VCO control data, since the frequency response characteristic of the PLL is corrected based upon the time constant of the loop filter, the stable C/N characteristic can be obtained irrespective of the VCO control data.

[0023] Then, the frequency synthesizer is featured by comprising: charge pump control means for outputting a signal used to vary a current capability of the charge pump in response to the output signal of the VCO control data producing means. With employment of such an arrangement, even when the control sensitivity of the VCO is varied in response to the VCO control data, since the frequency response characteristic of the PLL is corrected based upon the current capability of the charge pump, the stable C/N characteristic can be obtained irrespective of the VCO control data.

[0024] Also, the frequency synthesizer is featured by comprising: a reset signal generation means for outputting a signal which is synchronized with the output signal of the reference signal source to both a reset terminal of the first frequency divider and a reset terminal of the second frequency divider when the operation of the frequency adjusting means is commenced. With employment of such an arrangement, since the starting time instant of the frequency dividing operation by the first frequency divider can be made coincident with the starting time instant of the frequency dividing operation by the second frequency divider, the detection precision of the time difference detecting means can be furthermore improved.

[0025] Then, the frequency synthesizer is featured by comprising: a first delay means for delaying the clock signal of the first counter, or the clock signal of the second counter. With employment of such an arrangement, since the starting time instant of the frequency dividing operation by the first frequency divider can be made coincident with the starting time instant of the frequency dividing operation by the second frequency divider, the detection precision of the time difference detecting means can be furthermore improved.

[0026] Then, the frequency synthesizer is characterized by comprising: a second delay means for delaying the output signal of the reset signal generation means to output the delayed signal to both the reset terminal of the first frequency divider and the reset terminal of the second frequency divider. With employment of such an arrangement, since the time duration defined after the resonant circuit of the VCO has been switched until the frequency becomes stable can be secured, the frequency can be adjusted in higher precision.

[0027] Furthermore, according to the present invention, this frequency synthesizer is provided in a wireless mobile appliance. With employment of such an arrangement, it is possible to provide a compact wireless mobile appliance manufactured in low cost, while improving a communication quality thereof.

[0028] Then, according to the present invention, this frequency adjusting means 9 is provided in a wireless base station apparatus. With employment of such an arrangement, it is possible to provide a compact wireless base station apparatus made in low cost, while improving a communication quality thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029]

Fig. 1 is a block diagram for indicating a frequency synthesizer according to the present invention.

Fig. 2 is a block diagram for showing a frequency adjusting means employed in the frequency synthesizer according to the embodiment mode of the present invention.

Fig. 3 is a circuit diagram for representing a basic idea of a voltage-controlled oscillator employed in the frequency synthesizer according to the embodiment mode of the present invention.

Fig. 4 is a diagram for indicating a control voltage-to-oscillation frequency characteristic of the voltage-controlled oscillator employed in the frequency synthesizer of the embodiment mode of the present invention.
Fig. 5 is a block diagram of the conventional frequency synthesizer.
Fig. 6 is a circuit diagram for showing the basic idea of the voltage-controlled oscillator employed in the conventional frequency synthesizer.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0030] Referring now to drawings, various embodiment modes of the present invention will be described. It should be understood that the same reference numerals shown in the prior art of Fig. 5 and Fig. 6 will be employed as those for denoting the same, or similar constructive elements of a frequency synthesizer according to the present invention, and therefore, detailed description thereof are omitted.

[0031] Fig. 1 is a block diagram for representing a circuit arrangement of a frequency synthesizer according to the present invention. This frequency synthesizer is comprised of a frequency adjusting means 9 and a switch 10. In this frequency adjusting means 9, an output signal "f_{osc}" of a reference signal source 4, an output signal "f_{ref}" of a reference frequency divider 5, and an output signal "f_{div}" of a counter 3 are inputted to the frequency adjusting means. Also, a signal "CNT1" is outputted to the respective reset terminals of a prescaler 2, of a counter 3, and of the reference frequency divider 5. Another signal "CNT2" is outputted to a VCO 1, another signal "CNT3" is outputted to a loop filter 8, another signal "CNT4" is outputted to both a charge pump 7 and a switch 10, and a further signal "CNT5" is outputted to the charge pump 7 from this frequency adjusting means 9. The above-described switch 10 applies a voltage "V1" to the loop filter 8 in response to the signal CNT4.

[0032] Fig. 2 is a block diagram for indicating an arrangement of the frequency adjusting means 9. The output signal "f_{ref}" of the reference frequency divider 5 is inputted via a first delay means 907 to a counter 902, and the output signal "f_{div}" of the counter 3 is entered to a counter 903. Output signals produced in such a case that both the counter 902 and the counter 903 have accomplished the same numbers of counting operations are entered into a time difference detecting means 904, respectively. Also, the output signal "f_{osc}" of the reference signal source 4 is inputted to a reset signal generation means 901, and the reset signal generation means 901 outputs the signal "CNT1." An output signal "f_{ck}" of the prescaler 2 is inputted to the time difference detecting means 904 as a clock used to measure a time difference. The time difference detecting means 904 outputs a detection result of a time difference when the counting operation by the counter 902 is ended, and the counting operation by the counter 903 is ended to both a time difference judging means 910 and a VCO control data producing means 905. The time difference judging means 910 outputs a signal to a reset terminal of the counter 902 and a reset terminal of the counter 903, and also outputs a signal via a second delay means 909 to the reset signal generation means 901. A bias control means 908 outputs the signal CNT4 in response to the output signal of the time difference judging meas 910. The signal CNT2 outputted from the VCO control data producing means 905 is inputted to both a loop filter control means 906 and a charge pump control means 911, so that the loop filter control means 906 outputs the signal CNT3, and the charge pump control means 911 outputs the signal CNT5.

[0033] Fig. 3 is a structural diagram for showing a basic idea of the VCO 1. In this drawing, symbol "CNT2" indicates a bus line made by bundling CNT2-1 to CNT2-4. This VCO 1 owns such a technical different point from that shown in Fig. 6. That is, this VCO 1 shown in Fig. 3 is equipped with switches SW1 to SW4, which are controlled by the bus lines CNT2-1 to CNT2-4, and also capacitors C2 to C5, which are connected to these switches SW1 to SW4 in a cascade connection manner.

[0034] Fig. 4 is a graphical representation for representing a control voltage-to-oscillation frequency characteristic of the voltage-controlled oscillator shown in Fig. 3. Referring now to Fig. 4, operation of the voltage-controlled oscillator will be explained. It is now assumed that capacitance values of the variable capacitance diode "Cv" are equal to "Cv1" and "Cv2" when voltages "V1" and "V2" are applied to this variable capacitance diode Cv as the control voltage "Vt." In such a case that the control voltage Vt = V1 and all of the switches SW1 to SW4 are turned OFF (namely, characteristic 1 shown in Fig. 4), the oscillation frequency of this VCO is expressed by the following formula [2]:

$$f_{VCO} = 1/2\ \pi\sqrt{L[C0+C1 \cdot Cv1/(C1+Cv1)]} \qquad [2].$$

[0035] When the control voltage Vt = V2, and the switch SW1 is turned ON (namely, characteristic 2 of Fig. 4), the oscillation frequency is expressed by the below-mentioned formula [3]:

$$f_{VCO} = 1/2\ \pi\ \sqrt{L[C0+C2+C1 \cdot Cv2/(C1+Cv2)]} \qquad [3].$$

[0036] In order that the oscillation frequency defined in the formula [2] is made equal to that defined in the formula [3], using the following equation of:

[0037] $C1 \cdot Cv1 / (C1 + Cv1) = C2 + C2 - Cv2 / (C1 + Cv2)$, the capacitance value "C2" may be set to such a value defined by the below-mentioned formula [4]:

$$C2 = C1^2 (Cv1 - Cv2) / (C1 + Cv1)(C1 + Cv2) \quad [4].$$

[0038] While a similar study is made, in the case that the value of the capacitor is set to a value defined by the below-mentioned formula [5], when the switch SW2 is turned ON, a characteristics of Fig. 4 is obtained. Also, when the switches SW1 to SW3 are turned ON, a characteristic 4 of Fig. 4 is obtained. When the switches SW1 to SW4 are turned ON, a characteristic 5 of Fig. 4 is obtained.

$$C2=C3=C4=C5=C1^2(Cv1-Cv2)/(C1+Cv1)(C1+Cv2) \quad [5].$$

[0039] As a consequence, under control of the control voltage Vt and the bus lines CNT1 to CNT4, as represented in Fig. 4, the oscillation frequency is changed from "fL" when Vt = 0 up to "fH" when Vt = VH. In this case, the VCO 1 is assumed to be designed even when there are manufacturing fluctuations occurred in the electronic circuit elements which constitute the VCO 1, a desirable frequency is located within a frequency range from "fL" up to "fH."

[0040] Next, a description will now be made of operations of the frequency synthesizer shown in Fig. 1 and Fig. 2. When the count value of the counter 3 is changed which is set outside the frequency synthesizer, the reset signal generation means 901 generates the reset pulse CNT1 which is synchronized with the frequency "f_{OSC}", and then supplies this reset pulse CNT1 to the reference frequency divider 4, the prescaler 2, and the counter 3 so as to reset these circuit elements. At the same time, the bias control means 908 brings the output signal of the charge pump 7 to be brought into a high impedance state, and also applies the voltage V1 via the switch 10 to the output signal of the charge pump 7. At this time, the bias control means 908 turns ON the switches SW1 and SW2, so that the VCO 1 is oscillated at the frequency "f3."

[0041] As to the output signal "f_{ref}" of the reference frequency divider 4 and the output signal "f_{div}" of the counter 3, the counter 902 and the counter 903 count the same preselected numbers, respectively. When the counter 902 and the counter 903 accomplish the preselected count numbers respectively, these counters 902 and 903 output count end signals. At this time, since the frequency of the output signal "f_{ref}" is different from the frequency of the output signal "f_{div}", there is a difference between a count end time instant of the counter 902 and a count end time instant of the counter 903. The time difference detecting means 904 counts how many pulses of the output signals "f_{ck}" are produced from the prescaler 2 within this time difference. Since the oscillation frequency of the VCO 1 may be approximated based upon this count result at this stage, the VCO control data producing means 905 outputs as "CNT2", such control data capable of causing the VCO 1 to be oscillated at a target frequency. When the count value defined by the output signal "f_{ck}" of the prescaler 2 exceeds a predetermined value, the time difference judging means 910 resets both the counter 902 and the counter 903, and also supplies a signal via the delay means 909 to the reset signal generation means 901. Upon receipt of the signal supplied from the delay means 909, the reset signal generation means 901 outputs the signal "f_{OSC}" as CNT1 at this reception timing. As a result, this reset signal generation means 901 resets the reference frequency divider 5, the prescaler 2, and the counter 3, and then, commences to again perform the frequency adjusting operation.

[0042] While a similar process operation is repeatedly carried out, when a count value defined by the next output signal "f_{ck}" of the prescaler 2 is located within a preselected value, the time difference judging means 910 releases via the bias control means 908 the high impedance state of the output signal from the charge pump 7, and also releases applying of the voltage V1 via the switch 10 to the output of the charge pump 7. At this time, in response to the control data of the VCO control data producing means 905, the loop filter control means 906 switches the time constant of the loop filter 8. Also, in response to the control data outputted form the VCO control data producing means 905, the charge pump control means 911 switches the current capability of the charge pump 7. Thereafter, the frequency synthesizer is returned to the normal PLL operation, so that the frequency synthesizer is phase-locked.

[0043] It should be noted that there are four sets of resonant circuit switching units of the VCO 1 in the above-explained description. Alternatively, even when any other sets larger than, or smaller than the four sets are employed, the resonant circuit switching unit may be similarly realized. In particular, when a total number of these resonant circuit switching units is larger than 4, since the control sensitivity of the VCO per 1 stage can be lowered, the C/N characteristic may be improved. Also, in the above-explained description, the frequency of the resonant circuit is varied in such a manner that the switch is turned ON/OFF so as to connect, or disconnect the capacitor (fixed capacitance). Alternatively,

the resonant frequency may be varied in such a way that either the variable capacitance diodes or the inductors are connected, or disconnected. In other words, the resonant frequency may be varied by connecting, or disconnecting either the capacitors (fixed capacitances, variable capacitances) or the inductors.

[0044] As previously described, in accordance with the frequency synthesizer of this embodiment mode, even when there are the manufacturing fluctuations contained in the circuit elements which constitute the VCO 1, since the resonant frequency of the parallel resonant circuit is changed in response to the actual oscillation frequency of the VCO 1, this frequency synthesizer can be phase-locked at a desirable frequency. Moreover, since the VCO 1 can be manufactured in the IC form, the compact VCO 1 can be made in low cost.

[0045] Also, since the resonant circuits of the VCO 1 are switched by comparing the frequency of the output signal "f_{div}" with the frequency of the output signal "f_{ref}", the frequency synthesizer can be phase-locked at the desirable frequency even when the pulse-swallow type frequency divider is such a frequency divider in which the phase of the output signal is instantaneously changed. This frequency divider is employed in the generally known fractional N type frequency synthesizer.

[0046] Furthermore, since the PLL is set to the closed loop after such a confirmation is made such that the oscillation frequency of the VCO 1 is approximated to a desirable oscillation frequency, the frequency synthesizer can be phase-locked at this desirable frequency by employed in the optimum VCO control data.

[0047] Also, in order that the frequency changing time of the VCO 1 is eliminated which occurs just after the VCO control has been changed, the delay means 909 is inserted into the frequency synthesizer. As a result, the frequency can be adjusted in higher precision.

[0048] Furthermore, the time difference detecting means 904 is arranged in such a manner that the output signal "f_{ck}" is counted. Alternatively, the time difference detecting means 904 may be similarly realized by using such a signal obtained by multiplying the output signal of the reference signal source 4. In this alternative case, since the frequency of the signal to be counted is constant irrespective of the oscillation frequency of the VCO 1, the detection precision of the time difference can be continuously secured under stable condition.

[0049] Then, even when the control sensitivity of the VCO 1 is changed in response to the VCO control data, since the frequency response characteristic of the PLL is corrected based upon the time constant of the loop filter 8, the stable C/N characteristic can be obtained irrespective of the VCO control data.

[0050] Also, even when the control sensitivity of the VCO 1 is changed in response to the VCO control data, since the frequency response characteristic of the PLL is corrected based upon the current capability of the charge pump 7, the constant C/N characteristic can be obtained irrespective of the VCO control data. Since the correction by the current capability of the charge pump 7 may be realized by, for example, changing a total number of parallel transistors of the charge pump 7, the frequency response characteristic may be corrected in a more fine manner, as compared with the correction by employing the loop filter 8.

[0051] In addition, in such a case that the starting time instant of the frequency dividing operation by the reference frequency divider 5 is not made coincident with the starting time instant of the frequency dividing operation by the pulse-swallow type variable frequency divider which is constituted by the prescaler 2 and the counter 3, there is a shift between the end time instant of the counting operation of the counter 902 for counting the output signal "f_{div}" and the time instant of the counting operation of the counter 903 for counting the output signal "f_{ref}." As a consequence, in order to make the starting time instants of the frequency dividing operations coincident with each other, the reset signal CNT 1 is synthesized with the output signal "f_{OSC}." As a result, since the starting time instant of the frequency dividing operation by the reference frequency divider 5 can be made coincident with the time instant when the reset of the reference frequency divider 5 is released, the detection precision of the time difference detecting means 904 can be improved.

[0052] Also, precisely speaking, there is such an opportunity that a time instant when the reset signal CNT1 is inputted into the reference frequency divider 5 is not made coincident with a time instant when the reset signal CNT1 is entered into the prescaler 2. In the case that such time when the reset signal CNT1 is reached to the prescaler 2 is delayed, as compared with the time when the reset signal CNT1 is reached to the reference frequency divider 5, the signal "f_{ref}" entered into the counter 902 is delayed only by a difference between two sets of the propagation delay time. As a result, the propagation delay time error of the reset signal CNT1 is corrected, and the detection precision of the time difference detecting means 904 can be furthermore improved.

[0053] Also, in such a case that the frequency synthesizer of this embodiment mode is provided with the wireless mobile appliance, the compact wireless mobile appliance made in low cost can be realized with having the better communication quality.

[0054] Also, in such a case that the frequency synthesizer of this embodiment mode is provided with the wireless base station apparatus, the compact wireless base station apparatus made in low cost can be realized with having the better communication quality.

[0055] As previously described, in accordance with the present invention, it is possible to provide such a frequency synthesizer that the VCO having the better C/N characteristic and also the wide output frequency range can be man-

ufactured in the IC form and in low cost.

[0056] Also, since this frequency synthesizer is provided in the wireless mobile appliance and the wireless base station apparatus, it is possible to obtain the compact wireless mobile apparatus having the better communication quality and also the compact wireless base station apparatus having the better communication quality, which are made in low cost.

Claims

1. A frequency synthesizer comprising:

   a VCO (1), voltage-controlled oscillator, for generating an oscillating signal having a frequency related to a voltage applied to a control terminal of said VCO;

   a first frequency divider (3) for dividing the frequency of a signal derived from an output signal of said VCO;

   a second frequency divider (5) for dividing the frequency of a reference signal;

   a phase comparator (6) for comparing the phase of an output signal of said first frequency divider with the phase of an output signal of said second frequency divider to output a signal representative of the phase difference thereof;

   a charge pump (7) controlled by said phase difference signal for setting the voltage applied to the VCO control terminal;

   a loop filter (8) connected between the output of the charge-pump and the control terminal of said VCO;

   frequency adjusting means (9) for detecting a frequency error between said output signal of said first frequency divider and said output signal of said second frequency divider, and for switching the capacitor or the inductor value of said VCO in accordance with the result of the frequency error detection; and

   bias control means (10) for applying a voltage to said control terminal of said VCO so as to bring the output of said charge pump into a high impedance state when said frequency adjusting means is operated;

   characterized in that
   said frequency synthesizer further comprises:

   first and second counters (903, 902) for counting the output signal of said first frequency divider and the output signal of said second frequency divider as a clock;

   time difference detecting means (904) for detecting a time difference when the first counter produces a count end signal and the second counter produces a count end signal by employing a signal generated from the output signal of said VCO; and

   VCO control data producing means (905) for producing a signal used to switch the capacitor or the inductor value of said VCO in response to the output signal of said time difference detecting means.

2. A frequency synthesizer as claimed in claim 1 wherein said VCO (1) includes a plurality of means for switching capacitors or inductors.

3. A frequency synthesizer as claimed in any of claims 1 to 2, wherein said frequency synthesizer further comprises:

   time difference judging means (910) for resetting both said first counter (903) and said second counter (902) in response to the detection signal of said time difference detecting means (904), and for applying a voltage to said control terminal of said VCO so as to bring the output of said charge pump (7) into the high impedance state in the case that the time difference detected by said time difference detecting means (904) becomes a value defined within a predetermined time difference.

4. A frequency synthesizer as claimed in any of claims 1 to 3, wherein said frequency synthesizer further comprises:

loop filter control means (906) for outputting a signal causing a time constant of the loop filter (8) to be varied in response to the output signal of said VCO control data producing means (905).

5. A frequency synthesizer as claimed in any of claims 1 to 4, wherein said frequency synthesizer further comprises:

charge pump control means (911) for outputting a signal used to vary a current capability of said charge pump (7) in response to the output signal of said VCO control data producing means (905).

6. A frequency synthesizer as claimed in any of claims 1 to 5, wherein said frequency synthesizer further comprises:

reset signal generation means (901) for outputting a signal which is synchronized with the output signal of a reference signal source to both a reset terminal of said first frequency divider and a reset terminal of said second frequency divider when the operation of said frequency adjusting means (9) is commenced.

7. A frequency synthesizer as claimed in any of claims 1 to 6, wherein said frequency synthesizer further comprises.

first delay means (907) for delaying the clock signal of the first counter (903), or the clock signal of the second counter (902).

8. A frequency synthesizer as claimed in any of claims 1 to 7, wherein said frequency synthesizer further comprises:

second delay means (909) for delaying the output signal of said reset signal generation means (901) to output the delayed signal to both the reset terminal of said first frequency divider and the reset terminal of said second frequency divider.

9. A method for calibrating a frequency synthesizer comprising the steps of:

generating an oscillating signal with a VCO (1), voltage-controlled oscillator, having a frequency related to a voltage applied to a control terminal of said VCO;

dividing the frequency of a signal derived from an output signal of said VCO with a first frequency divider (3);

dividing the frequency of a reference signal with a second frequency divider (5);

comparing the phase of an output signal of said first frequency divider with the phase of an output signal of said second frequency divider and outputting a signal representative of the phase difference thereof;

controlling a charge pump (7) with said phase difference signal and outputting a voltage related to said phase difference signal;

filtering said voltage with a loop filter (8) and applying the filtered voltage to said control terminal of said VCO;

detecting a frequency error between said output signal of said first frequency divider and said output signal of said second frequency divider by means of frequency adjusting means (9), and switching the capacitor or the inductor value of said VCO in accordance with the result of the frequency error detection; and

applying a bias voltage to said control terminal of said VCO so as to bring the output of said charge pump into a high impedance state when said frequency adjusting means is operated;

characterized in that
said method for calibrating a frequency synthesizer further comprises the steps of:

counting the output signal of said first frequency divider and the output signal of said second frequency divider with a first and second counters (903, 902);

detecting a time difference when the first counter produces a count end signal and the second counter produces

a count end signal by employing a signal generated from the output signal of said VCO and time difference detecting means (904); and

producing a signal by means of VCO control data producing means (905) used to switch the capacitor or the inductor value of said VCO in response to the output signal of said time difference detecting means.

10. A method for calibrating a frequency synthesizer as claimed in claim 9, which further comprises a step of switching capacitors or inductors of said VCO (1).

11. A method for calibrating a frequency synthesizer as claimed in any of claims 9 to 10, which further comprises the steps of:

resetting both said first counter (903) and said second counter (902) in response to the detection signal of said time difference detecting means (904), and

applying a voltage to said control terminal of said VCO so as to bring the output of said charge pump (7) into the high impedance state in the case that the time difference detected by said time difference detecting means (904) becomes a value defined within a predetermined time difference.

12. A method for calibrating a frequency synthesizer as claimed in any of claims 9 to 11, which further comprises a step of generating a signal causing a time constant of the loop filter (8) to be varied in response to the output signal of said VCO control data producing means (905).

13. A method for calibrating a frequency synthesizer as claimed in any of claims 9 to 12, which further comprises a step of generating a signal used to vary a current capability of said charge pump (7) in response to the output signal of said VCO control data producing means (905).

14. A method for calibrating a frequency synthesizer as claimed in any of claims 9 to 13, which further comprises the steps of:

generating a signal with reset signal generation means (901) which is synchronized with said reference signal; and

outputting said signal which is synchronized with said reference signal to both a reset terminal of said first frequency divider and a reset terminal of said second frequency divider when the operation of said frequency adjusting means (9) is commenced.

15. A method for calibrating a frequency synthesizer as claimed in any of claims 9 to 14, which further comprises a step of delaying the clock signal of the first counter (903) or the clock signal of the second counter (902).

16. A method for calibrating a frequency synthesizer as claimed in any of claims 9 to 15, which further comprises a steps of delaying the output signal of said reset signal generation means (901) to output the delayed signal to both the reset terminal of said first frequency divider and the reset terminal of said second frequency divider.

17. A wireless mobile appliance comprising the frequency synthesizer as recited in any one of the preceding claims 1 to 8.

18. A wireless base station apparatus comprising the frequency synthesizer as recited in any one of the preceding claims 1 to 8.

Patentansprüche

1. Frequenzsynthesizer, der umfasst:

einen VCO (spannungsgesteuerten Oszillator) (1), der ein Schwingungssignal mit einer Frequenz erzeugt, die mit einer Spannung zusammenhängt, die an einen Steueranschluss des VCO angelegt wird;

einen ersten Frequenzteiler (3), der die Frequenz eines Signals teilt, das von einem Ausgangssignal des VCO hergeleitet wird;

einen zweiten Frequenzteiler (5), der die Frequenz eines Bezugssignals teilt;

einen Phasenkomparator (6), der die Phase eines Ausgangssignals des ersten Frequenzteilers mit der Phase eines Ausgangssignals des zweiten Frequenzteilers vergleicht, um ein Signal auszugeben, das die Phasendifferenz derselben darstellt;

eine Ladungspumpe (7), die von dem Phasendifferenzsignal gesteuert wird, um die an den VCO-Steueranschluss angelegte Spannung einzustellen;

ein Schleifenfilter (8), das zwischen den Ausgang der Ladungspumpe und den Steueranschluss des VCO geschaltet ist;

eine Frequenzreguliereinrichtung (9), die einen Frequenzfehler zwischen dem Ausgangssignal des ersten Frequenzteilers und dem Ausgangssignal des zweiten Frequenzteilers erfasst und den Kapazitäts- oder den Induktivitätswert des VCO entsprechend dem Ergebnis der Frequenzfehlererfassung schaltet; und

eine Vorspannungs-Steuereinrichtung (10), die eine Spannung an den Steueranschluss des VCO anlegt, um den Ausgang der Ladungspumpe in einen Hochimpedanzzustand zu versetzen, wenn die Frequenzregulier-einrichtung betrieben wird;

dadurch gekennzeichnet, dass:

der Frequenzsynthesizer des Weiteren umfasst:

einen ersten und einen zweiten Zähler (903, 902), die das Ausgangssignal des ersten Frequenzteilers und das Ausgangssignal des zweiten Frequenzteilers als einen Takt zählen;

eine Zeitdifferenz-Erfassungseinrichtung (904), die eine Zeitdifferenz erfasst, wenn der erste Zähler ein Zähl-Endsignal erzeugt und der zweite Zähler ein Zähl-Endsignal erzeugt, indem ein aus dem Ausgangssignal des VCO generiertes Signal benutzt wird; und

eine VCO-Steuerdaten-Erzeugungseinrichtung (905), die ein Signal erzeugt, das verwendet wird, um den Kapazitäts- oder den Induktivitätswert des VCO in Reaktion auf das Ausgangssignal der Zeitdifferenz-Erfassungseinrichtung zu schalten.

2. Frequenzsynthesizer nach Anspruch 1, wobei der VCO (1) eine Vielzahl von Einrichtungen zum Schalten von Kapazitäten oder Induktivitäten enthält.

3. Frequenzsynthesizer nach einem der Ansprüche 1 bis 2, wobei der Frequenzsynthesizer des Weiteren umfasst:

eine Zeitdifferenz-Feststelleinrichtung (910), die in Reaktion auf das Erfassungssignal der Zeitdifferenz-Erfassungseinrichtung (904) sowohl den ersten Zähler (903) als auch den zweiten Zähler (902) zurücksetzt und eine Spannung an den Steueranschluss des VCO anlegt, um den Ausgang der Ladungspumpe (7) in den Hochimpedanzzustand zu versetzen, wenn die von der Zeitdifferenz-Erfassungseinrichtung (904) erfasste Zeitdifferenz einen Wert annimmt, der innerhalb einer vorgegebenen Zeitdifferenz definiert ist.

4. Frequenzsynthesizer nach einem der Ansprüche 1 bis 3, wobei der Frequenzsynthesizer des Weiteren umfasst:

eine Schleifenfilter-Steuereinrichtung (906), die ein Signal ausgibt, das bewirkt, dass eine Zeitkonstante des Schleifenfilters (8) in Reaktion auf das Ausgangssignal von der VCO-Steuerdaten-Erzeugungseinrichtung (905) geändert wird.

5. Frequenzsynthesizer nach einem der Ansprüche 1 bis 4, wobei der Frequenzsynthesizer des Weiteren umfasst:

eine Ladungspumpen-Steuereinrichtung (911), die ein Signal ausgibt, das verwendet wird, um eine Stromka-

pazität der Ladungspumpe (7) in Reaktion auf das Ausgangssignal von der VCO-Steuerdaten-Erzeugungseinrichtung (905) zu ändern.

6. Frequenzsynthesizer nach einem der Ansprüche 1 bis 5, wobei der Frequenzsynthesizer des Weiteren umfasst:

eine Rücksetzsignal-Erzeugungseinrichtung (901), die ein Signal, das mit dem Ausgangssignal einer Bezugssignalquelle synchronisiert ist, sowohl an einen Rücksetzanschluss des ersten Frequenzteilers als auch einen Rücksetzanschluss des zweiten Frequenzteilers ausgibt, wenn der Betrieb der Frequenzreguliereinrichtung (9) begonnen wird.

7. Frequenzsynthesizer nach einem der Ansprüche 1 bis 6, wobei der Frequenzsynthesizer des Weiteren umfasst:

eine erste Verzögerungseinrichtung (907), die das Taktsignal des ersten Zählers (903) oder das Taktsignal des zweiten Zählers (902) verzögert.

8. Frequenzsynthesizer nach einem der Ansprüche 1 bis 7, wobei der Frequenzsynthesizer des Weiteren umfasst:

eine zweite Verzögerungseinrichtung (909), die das Ausgangssignal der Rücksetzsignal-Erzeugungseinrichtung (901) verzögert, um das verzögerte Signal sowohl an den Rücksetzanschluss des ersten Frequenzteilers als auch den Rücksetzanschluss des zweiten Frequenzteilers auszugeben.

9. Verfahren zum Kalibrieren eines Frequenzsynthesizers, das die folgenden Schritte umfasst:

Erzeugen eines Schwingungssignals mit einem VCO (spannungsgesteuerten Oszillator) (1), der eine Frequenz hat, die mit einer Spannung zusammenhängt, die an einen Steueranschluss des VCO angelegt wird;

Teilen der Frequenz eines Signals, das von einem Ausgangssignal des VCO hergeleitet wird, mit einem ersten Frequenzteiler (3);

Teilen der Frequenz eines Bezugssignals mit einem zweiten Frequenzteiler (5);

Vergleichen der Phase eines Ausgangssignals des ersten Frequenzteilers mit der Phase eines Ausgangssignals des zweiten Frequenzteilers und Ausgeben eines Signals, das die Phasendifferenz derselben darstellt;

Steuern einer Ladungspumpe (7) mit dem Phasendifferenzsignal und Ausgeben einer Spannung, die mit dem Phasendifferenzsignal zusammenhängt;

Filtern der Spannung mit einem Schleifenfilter (8) und Anlegen der gefilterten Spannung an den Steueranschluss des VCO;

Erfassen eines Frequenzfehlers zwischen dem Ausgangssignal des ersten Frequenzteilers und dem Ausgangssignal des zweiten Frequenzteilers mittels einer Frequenzreguliereinrichtung (9) und Schalten des Kapazitäts- oder des Induktivitätswertes des VCO entsprechend dem Ergebnis der Frequenzfehlererfassung; und

Anlegen einer Vorspannung an den Steueranschluss des VCO, um den Ausgang der Ladungspumpe in einen Hochimpetanzzustand zu versetzen, wenn die Frequenzreguliereinrichtung betrieben wird;

dadurch gekennzeichnet, dass:

das Verfahren zum Kalibrieren eines Frequenzsynthesizers des Weiteren die folgenden Schritte umfasst:

Zählen des Ausgangssignals des ersten Frequenzteilers und des Ausgangssignals des zweiten Frequenzteilers mit einem ersten und einem zweiten Zähler (903, 902);

Erfassen einer Zeitdifferenz, wenn der erste Zähler ein Zähl-Endsignal erzeugt und der zweite Zähler ein Zähl-Endsignal erzeugt, indem ein aus dem Ausgangssignal des VCO und der Zeitdifferenz-Erfassungseinrichtung (904) generiertes Signal benutzt wird; und

Erzeugen eines Signals mittels einer VCO-Steuerdaten-Erzeugungseinrichtung (905), das verwendet wird, um den Kapazitäts- oder den Induktivitätswert des VCO in Reaktion auf das Ausgangssignal der Zeitdifferenz-Erfassungseinrichtung zu schalten.

10. Verfahren zum Kalibrieren eines Frequenzsynthesizers nach Anspruch 9, das des Weiteren einen Schritt des Schaltens von Kapazitäten oder Induktivitäten des VCO (1) umfasst.

11. Verfahren zum Kalibrieren eines Frequenzsynthesizers nach einem der Ansprüche 9 bis 10, das des Weiteren die folgenden Schritte umfasst:

Zurücksetzen sowohl des ersten Zählers (903) als auch des zweiten Zählers (902) in Reaktion auf das Erfassungssignal der Zeitdifferenz-Erfassungseinrichtung (904), und

Anlegen einer Spannung an den Steueranschluss des VCO, um den Ausgang.der Ladungspumpe (7) in den Hochimpetanzzustand zu versetzen, wenn die von der Zeitdifferenz-Erfassungseinrichtung (904) erfasste Zeitdifferenz einen Wert annimmt, der innerhalb einer vorgegebenen Zeitdifferenz definiert ist.

12. Verfahren zum Kalibrieren eines Frequenzsynthesizers nach einem der Ansprüche 9 bis 11, das des Weiteren einen Schritt des Erzeugens eines Signals umfasst, das bewirkt, dass eine Zeitkonstante des Schleifenfilters (8) in Reaktion auf das Ausgangssignal der VCO-Steuerdaten-Erzeugungseinrichtung (905) geändert wird.

13. Verfahren zum Kalibrieren eines Frequenzsynthesizers nach einem der Ansprüche 9 bis 12, das des Weiteren einen Schritt des Erzeugens eines Signals umfasst, das verwendet wird, um eine Stromkapazität der Ladungspumpe (7) in Reaktion auf das Ausgangssignal der VCO-Steuerdaten-Erzeugungseinrichtung (905) zu ändern.

14. Verfahren zum Kalibrieren eines Frequenzsynthesizers nach einem der Ansprüche 9 bis 13, das des Weiteren die folgenden Schritte umfasst:

Erzeugen eines Signals, das mit dem Bezugssignal synchronisiert ist, mit einer Rücksetzsignal-Erzeugungseinrichtung (903); und

Ausgeben des Signals, das mit dem Bezugssignal synchronisiert ist, um sowohl einen Rücksetzanschluss des ersten Frequenzteilers als auch einen Rücksetzanschluss des zweiten Frequenzteilers zurückzusetzen, wenn der Betrieb der Frequenzreguliereinrichtung (9) begonnen wird.

15. Verfahren zum Kalibrieren eines Frequenzsynthesizers nach einem der Ansprüche 9 bis 14, das des Weiteren einen Schritt des Verzögems des Taktsignals des ersten Zählers (903) oder des Taktsignals des zweiten Zählers (902) umfasst.

16. Verfahren zum Kalibrieren eines Frequenzsynthesizers nach einem der Ansprüche 9 bis 15, das des Weiteren einen Schritt des Verzögems des Ausgangssignals der Rücksetzsignal-Erzeugungseinrichtung (901) umfasst, um das verzögerte Signal sowohl an den Rücksetzanschluss des ersten Frequenzteilers als auch den Rücksetzanschluss des zweiten Frequenzteilers auszugeben.

17. Drahtlos-Mobilgerät, das den Frequenzsynthesizer nach einem der vorangehenden Ansprüche 1 bis 8 umfasst.

18. Drahtlos-Basisstationsvorrichtung, die den Frequenzsynthesizer nach einem der vorangehenden Ansprüche 1 bis 8 umfasst.

Revendications

1. Synthétiseur de fréquences comprenant :

un oscillateur commandé en tension VCO (1), destiné à générer un signal périodique présentant une fréquence liée à une tension appliquée à une borne de commande dudit oscillateur VCO,
un premier diviseur de fréquence (3) destiné à diviser la fréquence d'un signal obtenue depuis un signal de sortie dudit oscillateur VCO,

un second diviseur de fréquence (5) destiné à diviser la fréquence d'un signal de référence,
un comparateur de phase (6) destiné à comparer la phase d'un signal de sortie dudit premier diviseur de fréquence à la phase d'un signal de sortie dudit second diviseur de fréquence afin de fournir en sortie un signal représentatif de leur différence de phase,
une pompe à charge (7) commandée par ledit signal de différence de phase destinée à établir la tension appliquée à la borne de commande de l'oscillateur VCO,
un filtre à boucle (8) relié entre la sortie de la pompe à charge et la borne de commande dudit oscillateur VCO,
un moyen de réglage de fréquence (9) destiné à détecter une erreur de fréquence entre ledit signal de sortie dudit premier diviseur de fréquence et ledit signal de sortie dudit second diviseur de fréquence, et destiné à commuter la valeur du condensateur ou de la bobine d'inductance dudit oscillateur VCO conformément au résultat de la détection de l'erreur de fréquence, et
un moyen de commande de polarisation (10) destiné à appliquer une tension à ladite borne de commande dudit oscillateur VCO de manière à amener la sortie de ladite pompe à charge dans un état de haute impédance lorsque ledit moyen de réglage de fréquence est actionné,

caractérisé en ce que
ledit synthétiseur de fréquences comprend en outre :

des premier et second compteurs (903, 902) destinés à compter le signal de sortie dudit premier diviseur de fréquence et le signal de sortie dudit second diviseur de fréquence en tant qu'horloge,
un moyen de détection de différence de temps (904) destiné à détecter une différence de temps lorsque le premier compteur produit un signal de fin de comptage et le second compteur fournit un signal de fin de comptage en employant un signal généré à partir du signal de sortie dudit oscillateur VCO, et
un moyen de production de données de commande d'oscillateur VCO (905) destiné à produire un signal utilisé pour commuter la valeur du condensateur ou de la bobine d'inductance dudit oscillateur VCO en réponse au signal de sortie dudit moyen de détection de différence de temps.

2. Synthétiseur de fréquences selon la revendication 1, dans lequel ledit oscillateur VCO (1) comprend une pluralité de moyens pour commuter les condensateurs ou les bobines d'inductances.

3. Synthétiseur de fréquences selon l'une quelconque des revendications 1 ou 2, dans lequel ledit synthétiseur de fréquences comprend en outre :

un moyen d'évaluation de différence de temps (910) destiné à réinitialiser à la fois ledit premier compteur (903) et ledit second compteur (902) en réponse au signal de détection dudit moyen de détection de différence de temps (904) et destiné à appliquer une tension à ladite borne de commande dudit oscillateur VCO de manière à amener la sortie de ladite pompe à charge (7) dans l'état de haute impédance dans le cas où la différence de temps détectée par ledit moyen de détection de différence de temps (904) devient une valeur définie dans les limites d'une différence de temps prédéterminée.

4. Synthétiseur de fréquences selon l'une quelconque des revendications 1 à 3, dans lequel ledit synthétiseur de fréquences comprend en outre :

un moyen de commande de filtre à boucle (906) destiné à fournir en sortie un signal amenant une constante de temps du filtre à boucle (8) à varier en réponse au signal de sortie dudit moyen de production de données de commande de l'oscillateur VCO (905).

5. Synthétiseur de fréquences selon l'une quelconque des revendications 1 à 4, dans lequel ledit synthétiseur de fréquences comprend en outre :

un moyen de commande de pompe à charge (911) destiné à fournir en sortie un signal utilisé pour faire varier une capacité en courant de ladite pompe à charge (7) en réponse au signal de sortie dudit moyen de production de données de commande d'oscillateur VCO (905).

6. Synthétiseur de fréquences selon l'une quelconque des revendications 1 à 5, dans lequel ledit synthétiseur de fréquences comprend en outre :

un moyen de génération de signal de réinitialisation (901) destiné à fournir en sortie un signal qui est synchro-

nisé avec le signal de sortie d'une source de signal de référence à la fois à une borne de réinitialisation dudit premier diviseur de fréquence et à une borne de réinitialisation dudit second diviseur de fréquence lorsque le fonctionnement dudit moyen de réglage de fréquence (9) est commencé.

7. Synthétiseur de fréquences selon l'une quelconque des revendications 1 à 6, dans lequel ledit synthétiseur de fréquences comprend en outre :

un premier moyen à retard (907) pour retarder le signal d'horloge du premier compteur (903) ou le signal d'horloge du second compteur (902).

8. Synthétiseur de fréquences selon l'une quelconque des revendications 1 à 7, dans lequel ledit synthétiseur de fréquences comprend en outre :

un second moyen à retard (909) destiné à retarder le signal de sortie dudit moyen de génération de signal de réinitialisation (901) afin de fournir en sortie le signal retardé à la fois à la borne de réinitialisation dudit premier diviseur de fréquence et à la borne de réinitialisation dudit second diviseur de fréquence.

9. Procédé d'étalonnage d'un synthétiseur de fréquences comprenant les étapes consistant à :

générer un signal périodique avec un oscillateur commandé en tension (1) VCO, présentant une fréquence liée à une tension appliquée à une borne de commande dudit oscillateur VCO,
diviser la fréquence d'un signal obtenue à partir d'un signal de sortie dudit oscillateur VCO par le biais d'un premier diviseur de fréquence (3),
diviser la fréquence d'un signal de référence avec un second diviseur de fréquence (5),
comparer la phase d'un signal de sortie dudit premier diviseur de fréquence à la phase d'un signal de sortie dudit second diviseur de fréquence et fournir en sortie un signal représentatif de leur différence de phase,
commander une pompe à charge (7) avec ledit signal de différence de phase et fournir en sortie une tension liée audit signal de différence de phase,
filtrer ladite tension avec un filtre à boucle (8) et appliquer la tension filtrée à ladite borne de commande dudit oscillateur VCO,
détecter une erreur de fréquence entre ledit signal de sortie dudit premier diviseur de fréquence et ledit signal de sortie dudit second diviseur de fréquence grâce à un moyen de réglage de fréquence (9) et commuter la valeur du condensateur ou de la bobine d'inductance dudit oscillateur VCO selon le résultat de la détection d'erreur de fréquence, et
appliquer une tension de polarisation à ladite borne de commande dudit oscillateur VCO de manière à amener la sortie de ladite pompe à charge dans un état de haute impédance lorsque ledit moyen de réglage de fréquence est actionné,

caractérisé en ce que
ledit procédé destiné à étalonner un synthétiseur de fréquences comprend en outre les étapes consistant à :

compter le signal de sortie dudit premier diviseur de fréquence et le signal de sortie dudit second diviseur de fréquence avec des premier et second compteurs (903, 902),
détecter une différence de temps lorsque le premier compteur produit un signal de fin de comptage et le second compteur produit un signal de fin de comptage en employant un signal généré à partir du signal de sortie dudit oscillateur VCO et dudit moyen de détection de différence de temps (904), et
produire un signal au moyen d'un moyen de production de données de commande d'oscillateur VCO (905) utilisé pour commuter la valeur du condensateur ou de la bobine d'inductance de l'oscillateur VCO en réponse au signal de sortie dudit moyen de détection de différence de temps.

10. Procédé d'étalonnage de synthétiseur de fréquences selon la revendication 9, qui comprend en outre une étape consistant à commuter les condensateurs ou les bobines d'inductances dudit oscillateur VCO (1).

11. Procédé d'étalonnage d'un synthétiseur de fréquences selon l'une quelconque des revendications 9 à 10, qui comprend en outre les étapes consistant à :

réinitialiser à la fois ledit premier compteur (903) et ledit second compteur (902) en réponse au signal de détection dudit moyen de détection de différence de temps (904), et

appliquer une tension à ladite borne de commande dudit oscillateur VCO de manière à amener la sortie de ladite pompe à charge (7) dans l'état de haute impédance dans le cas où la différence de temps détectée par ledit moyen de détection de différence de temps (904) devient une valeur définie dans les limites d'une différence de temps prédéterminée.

12. Procédé d'étalonnage d'un synthétiseur de fréquences selon l'une quelconque des revendications 9 à 11, qui comprend en outre une étape consistant à générer un signal amenant une constante de temps du filtre à boucle (8) à varier en réponse au signal de sortie dudit moyen de production de données de commande d'oscillateur VCO (905).

13. Procédé d'étalonnage d'un synthétiseur de fréquences selon l'une quelconque des revendications 9 à 12, qui comprend en outre une étape consistant à générer un signal utilisé pour faire varier une capacité en courant de ladite pompe à charge (7) en réponse au signal de sortie dudit moyen de production de données de commande d'oscillateur VCO (905).

14. Procédé d'étalonnage d'un synthétiseur de fréquences selon l'une quelconque des revendications 9 à 13, qui comprend en outre les étapes consistant à :

générer un signal avec un moyen de génération de signal de réinitialisation (901) qui est synchronisé avec ledit signal de référence, et
fournir en sortie ledit signal qui est synchronisé avec ledit signal de référence à la fois à une borne de réinitialisation dudit premier diviseur de fréquence et à une borne de réinitialisation dudit second diviseur de fréquence lorsque le fonctionnement dudit moyen de réglage de fréquence (9) est commencé.

15. Procédé d'étalonnage d'un synthétiseur de fréquences selon l'une quelconque des revendications 9 à 14, qui comprend en outre une étape consistant à retarder le signal d'horloge du premier compteur (903) ou le signal d'horloge du second compteur (902).

16. Procédé d'étalonnage d'un synthétiseur de fréquences selon l'une quelconque des revendications 9 à 15, qui comprend en outre une étape consistant à retarder le signal de sortie dudit moyen de génération de signal de réinitialisation (901) afin de fournir en sortie le signal retardé à la fois à la borne de réinitialisation dudit premier diviseur de fréquence et à la borne de réinitialisation dudit second diviseur de fréquence.

17. Appareil mobile sans fil comprenant le synthétiseur de fréquences selon l'une quelconque des revendications précédentes 1 à 8.

18. Dispositif de station de base sans fil comprenant un synthétiseur de fréquences selon l'une quelconque des revendications 1 à 8.

FIG. 1

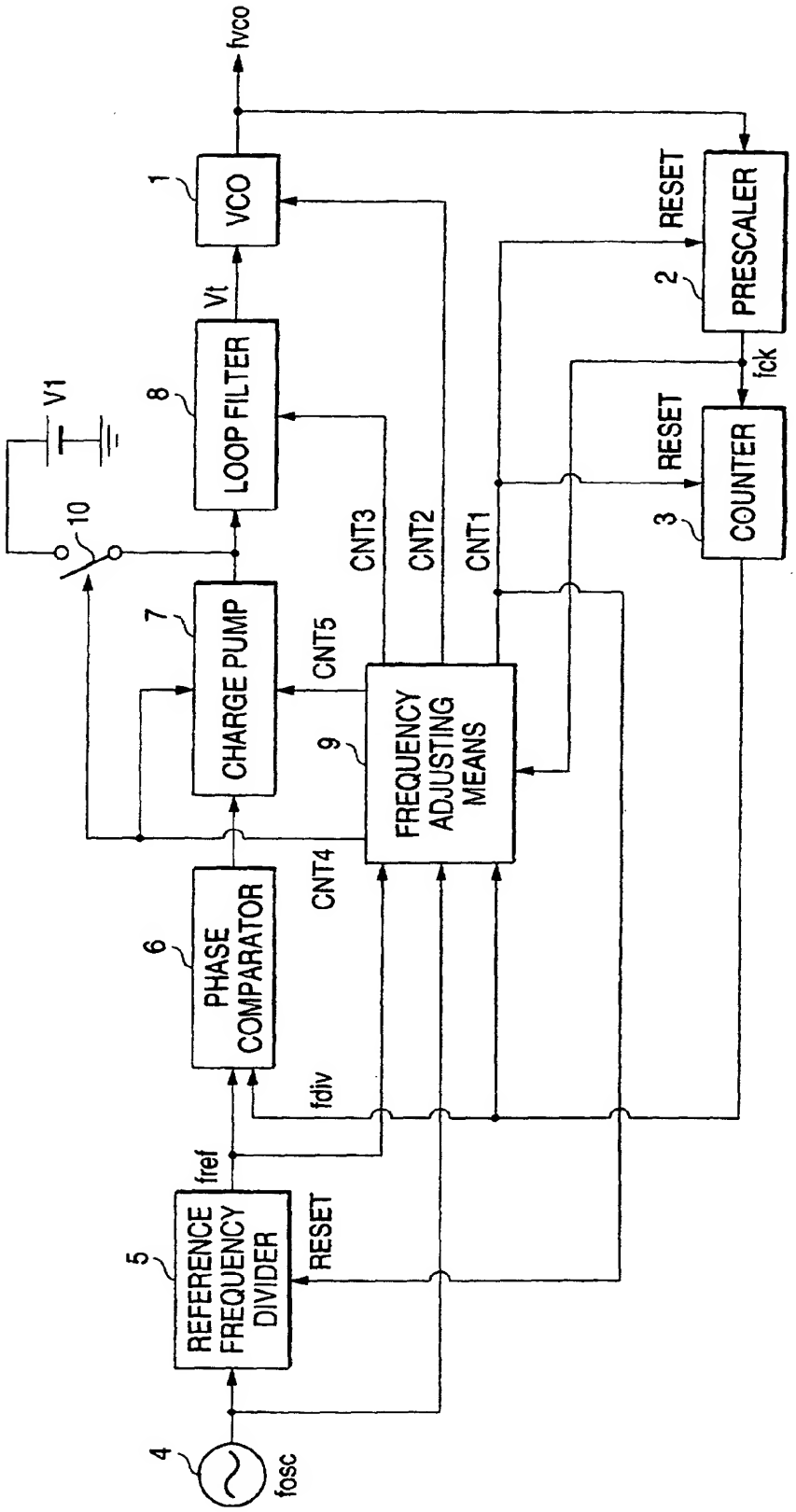

fvco
1
VCO
Vt
8
LOOP FILTER
V1
10
7
CHARGE PUMP
CNT5
9
FREQUENCY ADJUSTING MEANS
CNT3
CNT2
CNT1
CNT4
6
PHASE COMPARATOR
fdiv
fref
5
REFERENCE FREQUENCY DIVIDER
RESET
4
fosc
RESET
2
PRESCALER
fck
RESET
3
COUNTER

FIG. 2

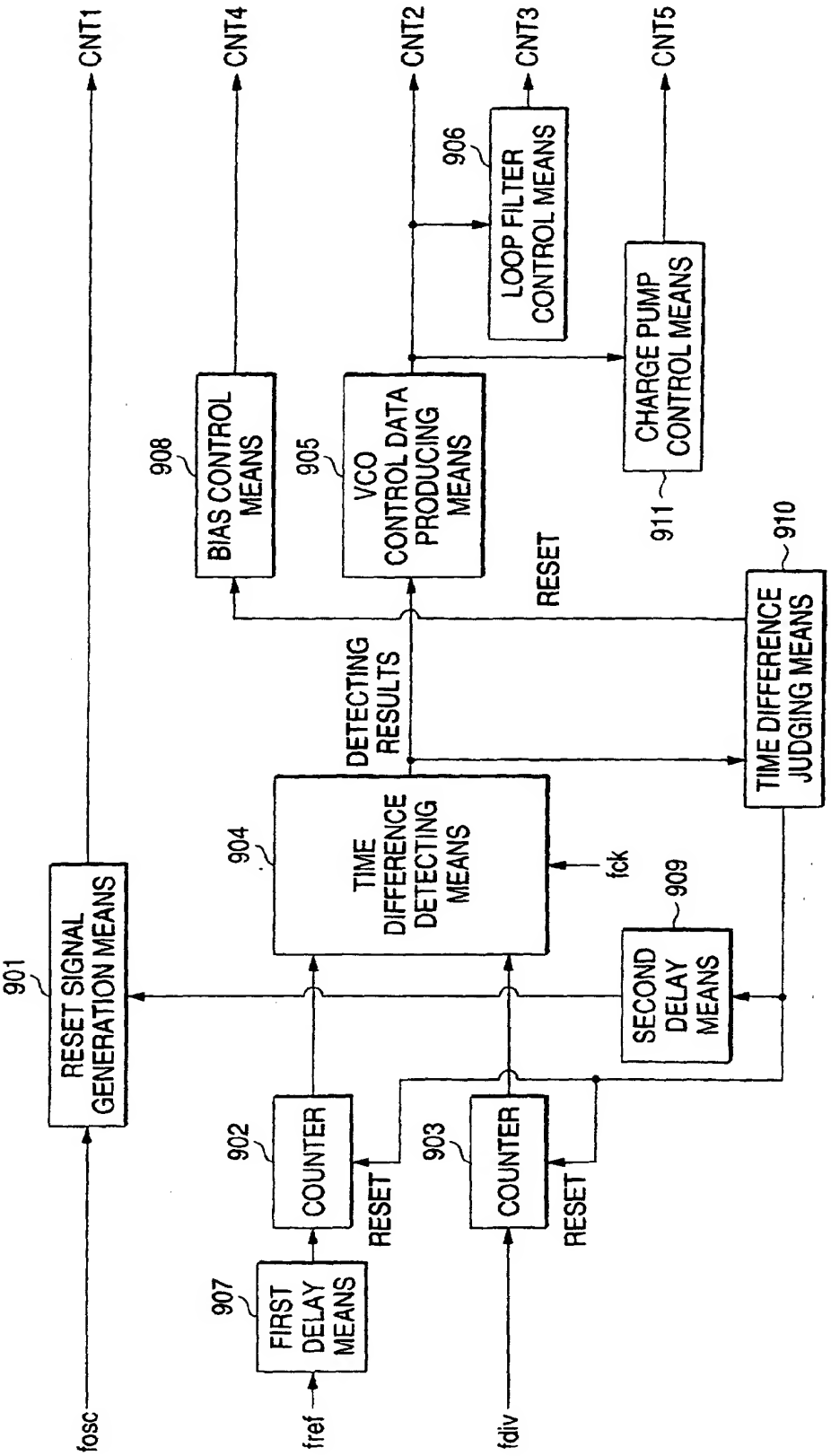

CNT1
CNT4
CNT2
CNT3
CNT5
906
LOOP FILTER CONTROL MEANS
908
BIAS CONTROL MEANS
905
VCO CONTROL DATA PRODUCING MEANS
CHARGE PUMP CONTROL MEANS
911
RESET
910
DETECTING RESULTS
TIME DIFFERENCE JUDGING MEANS
904
TIME DIFFERENCE DETECTING MEANS
fck
909
SECOND DELAY MEANS
901
RESET SIGNAL GENERATION MEANS
902
COUNTER
903
COUNTER
RESET
RESET
907
FIRST DELAY MEANS
fosc
fref
fdiv

FIG. 3

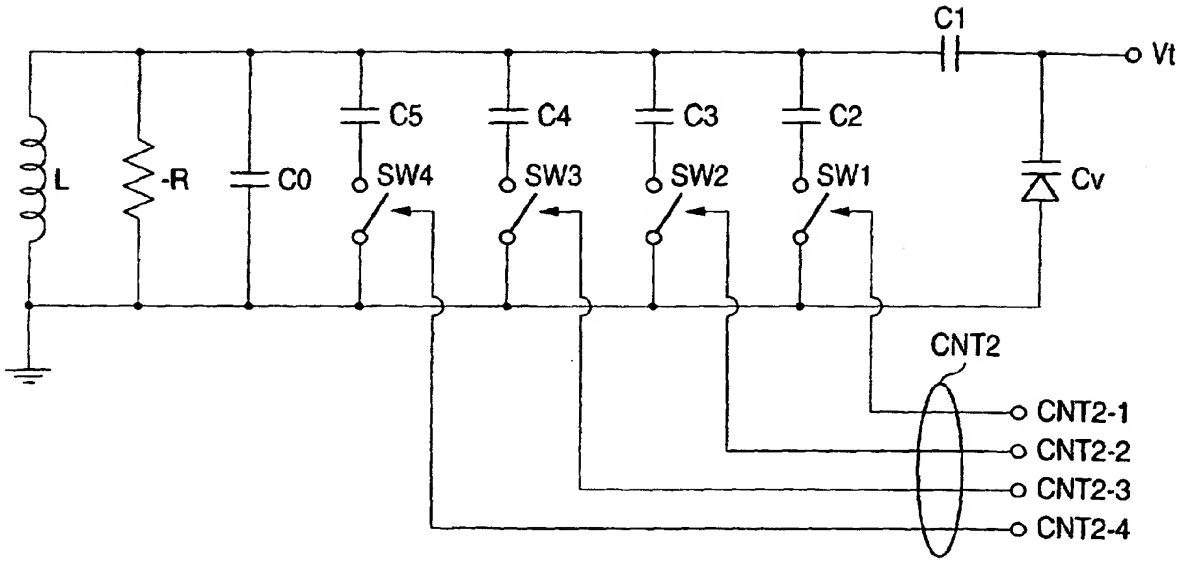

C1
Vt
L
-R
C0
C5
C4
C3
C2
SW4
SW3
SW2
SW1
Cv
CNT2
CNT2-1
CNT2-2
CNT2-3
CNT2-4

FIG. 4

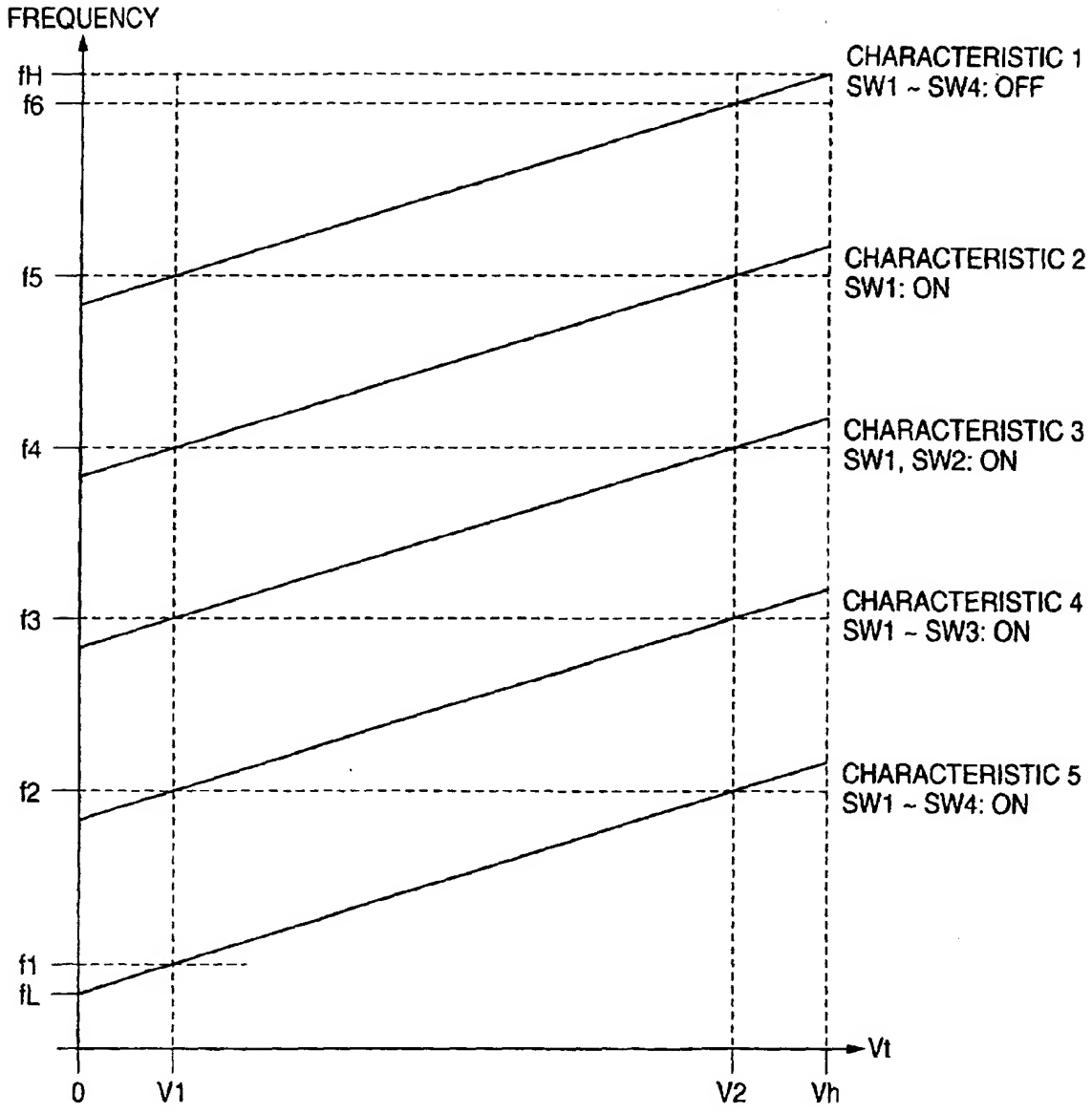

FREQUENCY
fH
f6
f5
f4
f3
f2
f1
fL
0
V1
V2
Vh
Vt
CHARACTERISTIC 1
SW1 ~ SW4: OFF
CHARACTERISTIC 2
SW1: ON
CHARACTERISTIC 3
SW1, SW2: ON
CHARACTERISTIC 4
SW1 ~ SW3: ON
CHARACTERISTIC 5
SW1 ~ SW4: ON

FIG. 5

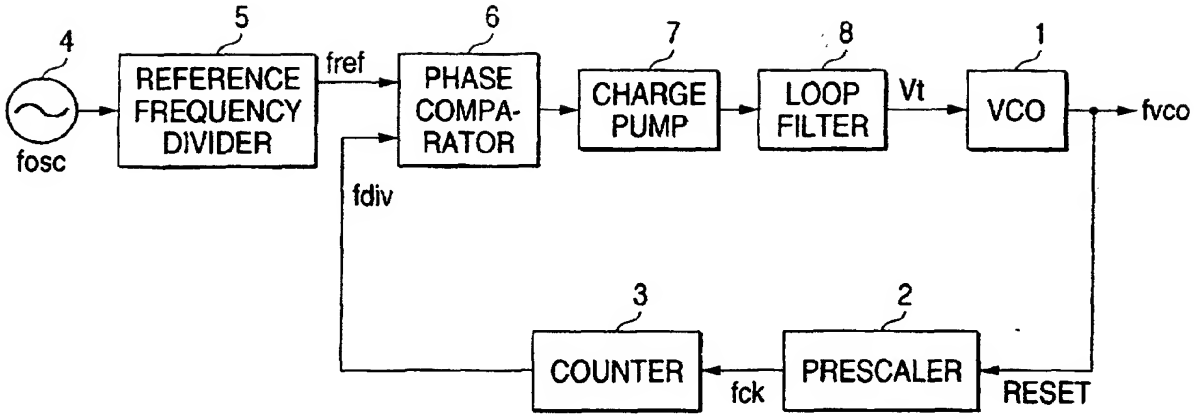
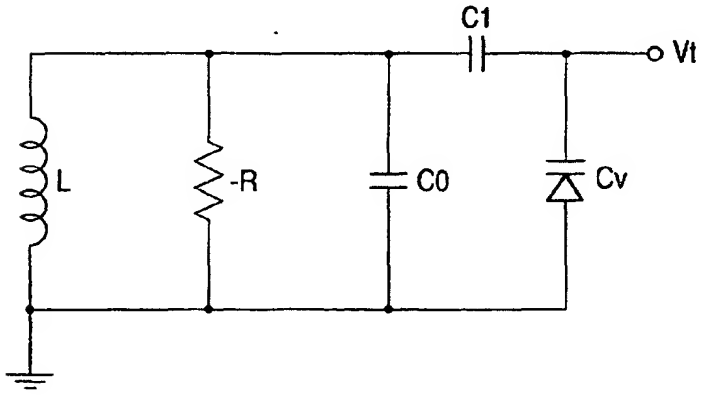

4
5
6
7
8
1
REFERENCE FREQUENCY DIVIDER
fref
PHASE COMPA-RATOR
CHARGE PUMP
LOOP FILTER
Vt
VCO
fvco
fosc
fdiv
3
2
COUNTER
fck
PRESCALER
RESET

FIG. 6


C1
Vt
L
-R
C0
Cv